Solution:

$$F = \Sigma(1, 2, 3, 4, 8)$$

a) Decoder

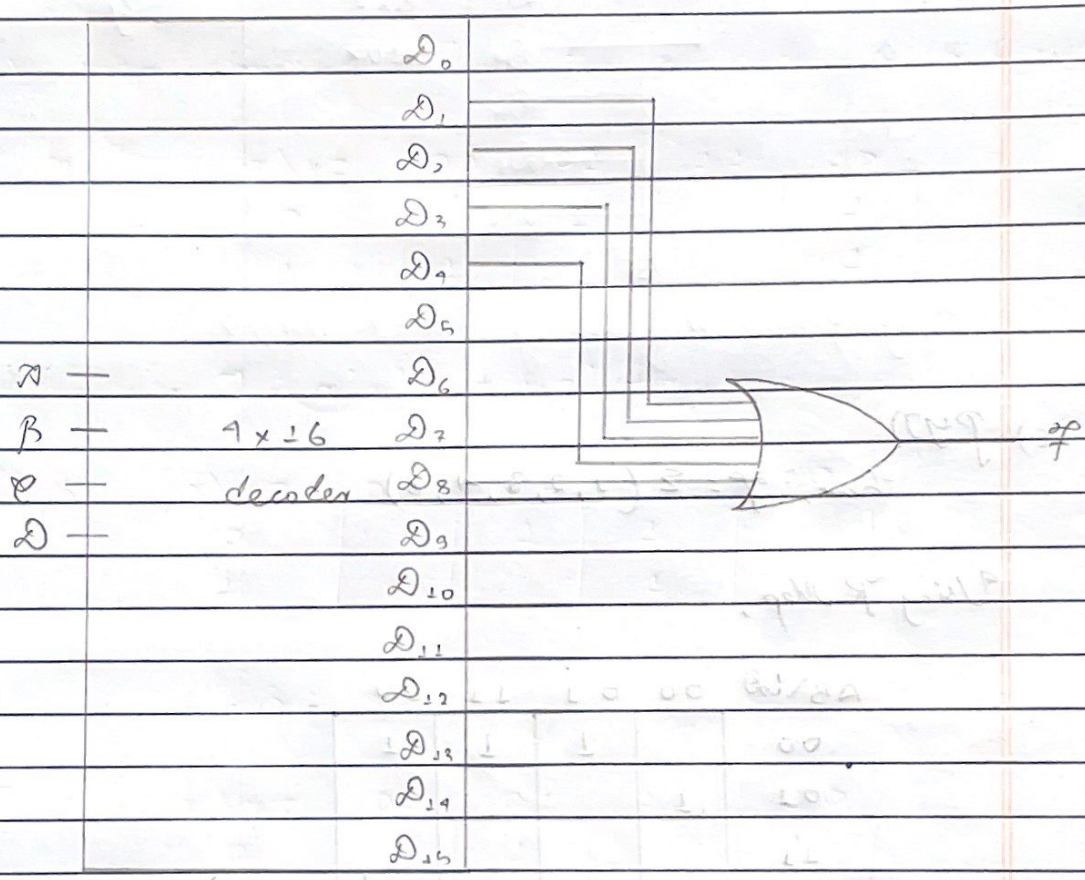


Fig Implementation of F using 4x16 Decoder

b) Multiplexer:

Let A be the input lines and B, C & D be selection lines.

Implementing with 8:1 MUX, we get,

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
A'	0	(1)	(2)	(3)	(4)	5	6	7
A	(8)	9	10	11	12	13	14	15
	A	A'	A'	A'	A'	0	0	0

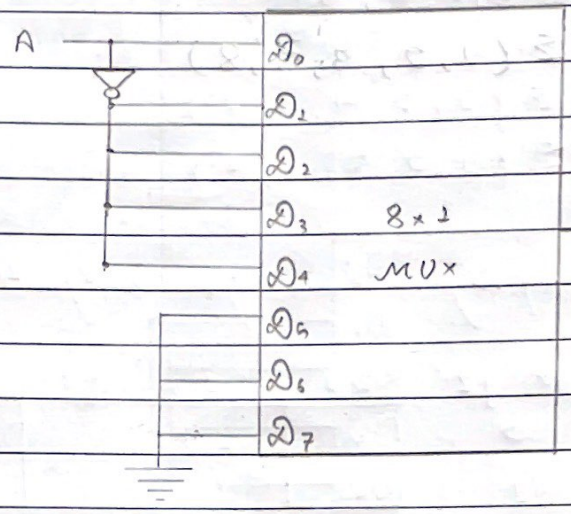


Fig. Block diagram of 8:1 MUX

c) PyD:

here, $F = \Sigma(1,2,3,4,8)$

Using K Map,

AB\CD	00	01	11	10
00		1	1	1
01	1			
11				
10	1			

$\therefore F = A'B'C + A'B'CD + A'BC'D' + AB'C'D'$

Here,

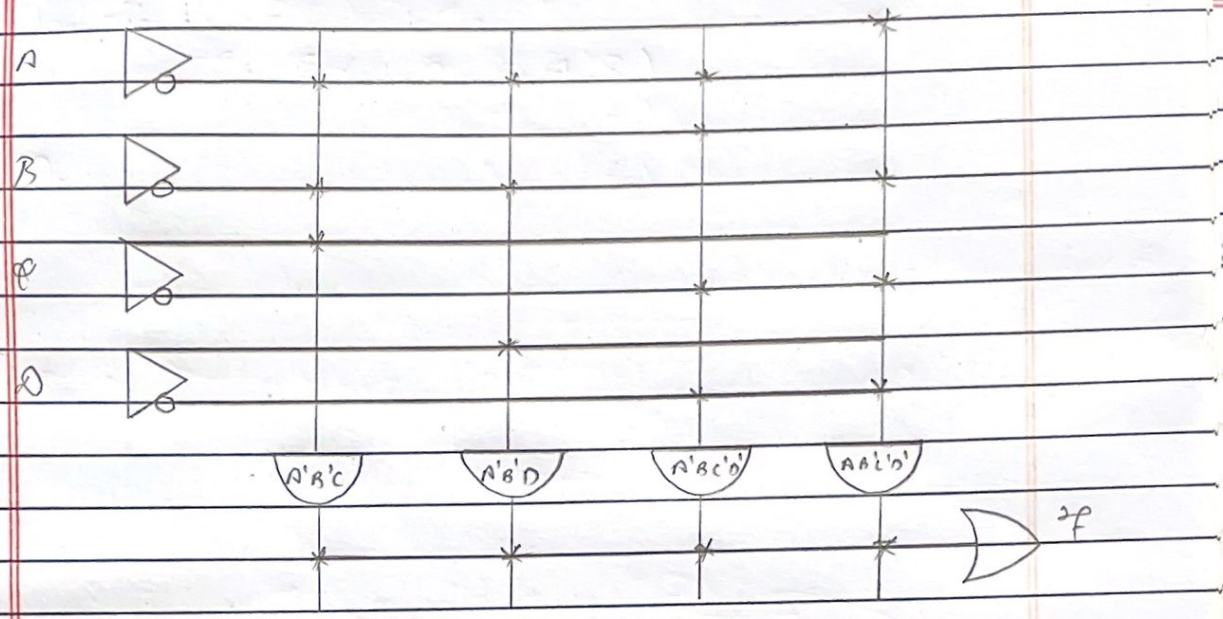
No. of input buffer = 3 (i.e. A, B, C, D)

No. of programmable AND gate

= No. of min-terms = 4

No. of programmable OR gate

= No. of output functions = 1


A
B
C
D
y
A'B'C
A'B'D
A'BC'D'
ABC'D'
f